

# PATENT APPLICATION

## GLITCH FREE RESET CIRCUIT

INVENTORS: Sarathy Sribhashyam  
3196 Whitesand Drive  
San Jose, CA 95148  
Citizenship: INDIA

DAVID HOFF  
1667 Four Oakds Road  
San Jose, CA 95131  
Citizenship: U.S.A.

KEN MING LI  
3454 Notre Dame Drive  
Santa Clara, CA 95051  
Citizenship: TAIWAN

LARGE ENTITY

SQUIRE, SANDERS & DEMPSEY L.L.P.  
600 Hansen Way  
Palo Alto, CA 94304-1043  
(650) 856-6500

Express Mail Label No.: **EL 701 363 411 U.S.**

1                    GLITCH FREE RESET CIRCUIT

2                    Inventors: Sarathy Sribhashyam

3                    David Hoff

4                    Ken Ming Li

5  
6                    TECHNICAL FIELD

7                    This disclosure relates generally to integrated circuits  
that are used in, for example, computing devices, and more  
particularly but not exclusively, to circuits and methods that  
solve the problem of glitches occurring in a reset signal that is  
applied to an integrated circuit on a circuit board. The present  
invention also relates more particularly to circuits and methods  
that enhance the operation of integrated circuits.

10  
11  
12  
13  
14  
15  
16                    BACKGROUND

17                    When an integrated circuit (i.e., a chip or part) is on a  
18 circuit board, the reset signal applied to the integrated circuit  
19 usually has glitches, and these glitches can lock up the  
20 integrated circuit, as well as prevent the integrated circuit  
21 from functioning. Thus, it is desirable to eliminate such  
22 glitches from the reset signals and enhance the operation of the  
23 integrated circuit. Conventionally, a glitch free reset signal  
24 is obtained from the circuit board. In conventional approaches,  
25 emphasis was typically placed on eliminating such glitches on the  
reset signals that are applied to the integrated circuit.

1 However, as the number of cards on the circuit board increases,  
2 the likelihood of completely eliminating a glitch in a reset  
3 signal from the circuit board decreases. Accordingly,  
4 improvements are needed with regard to solving the problem of  
5 glitches that occur in reset signals that are applied to  
6 integrated circuits.

7

#### BRIEF DESCRIPTION OF THE DRAWINGS

8 Non-limiting and non-exhaustive embodiments of the present  
9 invention are described with reference to the following figures,  
10 wherein like reference numerals refer to like parts throughout  
11 the various views unless otherwise specified.

12 Figure 1 is a block diagram of a system that is typically  
13 implemented in, for example, a personal computer.

14 Figure 2 is a waveform diagram of a reset signal in ideal  
15 form and a waveform diagram of a practical reset signal that  
16 includes a glitch.

17 Figure 3 is a schematic block diagram of a system that is  
18 capable of compensating for glitches in a reset signal, in  
19 accordance with an embodiment of the present invention.

20 Figure 4 is a schematic circuit diagram of one embodiment  
21 of the reset circuit of Figure 3.

22 Figure 5 illustrates various example waveform diagrams of  
23 the signals that are processed in the reset circuit of Figure 4,  
24

1 with the incoming reset signal (GFRST\_IN0) shown as switching to  
2 a high state.

3 Figure 6 illustrates various example waveform diagrams of  
4 the signals that are processed in the reset circuit of Figure 4,  
5 with the incoming reset signal (GFRST\_IN0) shown as switching to  
6 a low state.

7 Figure 7 illustrates various example waveform diagrams  
including the incoming reset signals with glitch occurrences and  
the complete output reset signal generated by a reset circuit in  
accordance with an embodiment of the present invention.

8 Figure 8 is a flowchart diagram of a method of compensating  
for glitch occurrence in an incoming reset signal, in accordance  
with an embodiment of the present invention.

9 Figure 9 is a schematic circuit diagram of a second  
10 embodiment of the reset circuit of Figure 3.

11 Figure 10 illustrates various example waveform diagrams of  
12 the signals that are processed by the reset circuit of Figure 9.

13 Figure 11 is a flowchart diagram of a method of  
14 compensating for glitch occurrence in an incoming reset signal,  
15 in accordance with another embodiment of the present invention.

21

1 DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

2       Embodiments of systems and methods for compensating for a  
3 glitch occurrence in a reset signal are disclosed herein. As an  
4 overview, an embodiment of the invention provides a reset  
5 circuit that compares an original reset signal with a delayed  
6 version of the reset signal. When the reset circuit detects  
7 both the original non-delayed reset signal and the delayed  
version of the reset signal to be in the same state, then that  
state (which is output from an S-R flop) is applied to the  
appropriate components of an integrated circuit.

8       In another embodiment, a reset circuit receives an incoming  
9 reset signal "reset" and delays an incoming reset signal to  
10 generate a delayed reset signal "delayed\_reset". The reset  
11 circuit compares the non-delayed reset signal with the  
12 delayed\_reset signal. When both the non-delayed reset signal and  
13 the delayed\_reset signal are in the same state (asserted state or  
14 non-asserted state), then the non-delayed reset signal is sampled  
15 as the output value "OUTB". On the other hand, if the non-  
16 delayed reset signal and the delayed\_reset signal are not in the  
17 same state, then the non-delayed reset signal is not sampled, and  
18 the previously sampled state of the non-delayed reset signal is  
19 held as the output value "OUTB". The output value "OUTB"  
20 determines the value of the reset signal that is applied to the  
21 appropriate components of an integrated circuit.

1       The present invention advantageously solves the problem of  
2 glitch occurrences in reset signals that are applied to  
3 integrated circuits. The present invention also advantageously  
4 provides circuits and methods that are very versatile and that  
5 may be selectively used anywhere on the circuit board to  
6 eliminate glitches in signals. The present invention may also  
7 advantageously provide circuits and methods that effectively  
8 eliminate small glitches in reset signals by minimizing the  
9 signal delay and that effectively eliminate larger glitches in  
10 reset signals by increasing the signal delay. Thus, the present  
11 invention may advantageously enhance the operation of integrated  
12 circuits on a circuit board.

13       In the description herein, numerous specific details are  
14 provided, such as the description of system components in  
15 Figures 1 through 11, to provide a thorough understanding of  
16 embodiments of the invention. One skilled in the relevant art  
17 will recognize, however, that the invention can be practiced  
18 without one or more of the specific details, or with other  
19 systems, methods, components, materials, parts, and/or the like.  
20 In other instances, well-known structures, materials, or  
21 operations are not shown or described in detail to avoid  
22 obscuring aspects of the invention.

23       Reference throughout this specification to "one  
24 embodiment", "an embodiment", or "a specific embodiment" means

1 that a particular feature, structure, or characteristic  
2 described in connection with the embodiment is included in at  
3 least one embodiment of the present invention. Thus, the  
4 appearances of the phrases "in one embodiment", "in an  
5 embodiment", or "in a specific embodiment" in various places  
6 throughout this specification are not necessarily all referring  
7 to the same embodiment. Furthermore, the particular features,  
structures, or characteristics may be combined in any suitable  
manner in one or more embodiments.

Additionally, the signal arrows in the drawings/figures are  
considered as exemplary and are not limiting, unless otherwise  
specifically noted. Furthermore, the term "or" as used in this  
disclosure is generally intended to mean "and/or" unless  
otherwise indicated. Combinations of components or steps will  
also be considered as being noted, where terminology is foreseen  
as rendering the ability to separate or combine is unclear.

17 It will also be appreciated that one or more of the  
18 elements depicted in the drawings/figures can also be  
19 implemented in a more separated or integrated manner, or even  
20 removed or rendered as inoperable in certain cases, as is useful  
21 in accordance with a particular application.

22 Referring in detail now to the drawings wherein similar  
23 parts of the present invention are identified by like reference  
24 numerals, and initially referencing Figure 1 as a preamble for

1 better understanding the need for the present invention, there  
2 is seen a block diagram of a conventional system 100 including a  
3 chipset 105, central processing unit (CPU) 110, memory 115,  
4 southbridge 120, graphics chip 125, and audio chip (or other  
5 type of chip) 130. The system 100 may or may not include the  
6 graphics chip 125 or audio chip 130. Other types of chips may  
7 also be included (or may instead be included) in the system 100.

The conventional system 100 is of the type that may be implemented in, for example, a personal computer (PC). The chipset 105, graphics chip 125, and audio chip 130 are coupled together by a bus 135 such as, for example, a peripheral component interconnect (PCI) bus.

As known to those skilled in the art, a chipset is a number of integrated circuits designed to perform one or more related functions. For example, one chipset may provide the basic functions of a modem while another chipset provides the central processing unit (CPU) functions for a computer. Newer chipsets generally include functions provided by two or more older-type chipsets. In some cases, older-type chipsets that require two or more physical chips can be replaced with a chipset on one chip. The chipset 105 communicates with the CPU 110, memory 115, and southbridge 120. The CPU 110 can only communicate directly with the chipset 105. Thus, if the CPU 110 will retrieve data from the memory 115, the CPU 110 will instruct the



1 chipset 105 to retrieve the data from memory 115, and data is  
2 then transferred by the chipset 105 from the memory 115 to the  
3 CPU 110. Similarly, if the graphics chip 125 or audio chip 130  
4 will retrieve data from the memory 115, the graphics chip 125 or  
5 audio chip 130 will instruct the chipset 105 to retrieve the  
6 data from memory 115, and data is then transferred by the  
7 chipset 105 from the memory 115 to the graphics chip 125 or  
audio chip 130.

The chipset 105 may be of the type available from, for example, Via Technology, Incorporated, Fremont, California or Intel Corporation, Santa Clara, California. The CPU 110 may be of the type available from, for example, Intel Corporation or Motorola Incorporated. The memory 115 may be, for example, a dynamic random access memory (DRAM) for serving as a main memory device.

16 As known to those skilled in the art, a southbridge is the  
17 integrated circuit in a core logic chip set that controls the  
18 integrated drive electronics (IDE) bus, universal serial bus  
19 (USB), plug-n-play support, the Peripheral Component  
20 Interconnect Industry Standard Architecture (PCI-ISA) bridge,  
21 keyboard/mouse controller, power management, and various other  
22 features. One particular southbridge brand provides sound card  
23 functions.

1 The graphics chip 125 may be of the type available from,  
2 for example, S3 Graphics, Incorporated, Fremont, California,  
3 while the audio chip 130 may be of the type available from  
4 various manufacturers.

5 As also known to those skilled in the art, a PCI bus is a  
6 local bus standard developed by Intel Corporation. Most modern  
7 personal computers include a PCI bus in addition to a more  
general ISA expansion bus. PCI is also used on newer versions  
of the Macintosh computer from Apple Computers Corporation,  
Cupertino, California.

8 The chipset 105 sends a reset signal 140 via bus 135 to the  
9 graphics chip 125, audio chip 130, and other chips coupled to  
10 the bus 135 before the chipset 105 begins communication with  
11 these chips. However, in practice, since multiple chips (e.g.,  
12 graphics chip 125 and audio chip 130) share the bus 135, the  
13 reset signal 140 will not be smooth in form and will include a  
14 glitch that adversely impacts the operation of the system 100.  
15 In this conventional system 100, components are typically used  
16 to try to eliminate glitch occurrence in the reset signal.  
17 However, as number of integrated circuits on the circuit board  
18 increases, the likelihood of completely eliminating a glitch in a  
19 reset signal 140 decreases.

20 Figure 2 shows a waveform diagram of a reset signal 140a  
21 (generated by chipset 105) in ideal form. The reset signal 140a  
22

1 may typically not include any glitches if multiple integrated  
2 circuits do not share the bus 135.

3 Figure 2 also shows a waveform diagram of a reset signal  
4 140b which is generated by the chipset 105 in practical  
5 implementations. The reset signal 140b includes a glitch 200  
6 that is the result of a multiple number of integrated circuits  
7 sharing the bus 135. Typically, the glitch 200 detrimentally  
8 triggers the reset on some parts of the graphics chip 125 and/or  
9 on some part of the other integrated circuits that share the bus  
10 135. Since the glitch 200 appears at a high level for only a  
11 very short time frame, the reset that is triggered by the glitch  
12 200 is only applied to a part of the graphics chip 125 and is  
13 not applied to the entirety of the graphics chip 125. As a  
14 result, when the actual reset 205 is received by graphics chip  
15 125, reset is again triggered in graphics chip 125. This  
16 results in the graphics chip 125 in becoming locked (crashing)  
17 because some components in graphics chip 125 have already been  
18 reset by the previous glitch 200, while some components in  
19 graphics chip 125 have not been reset by glitch 200. This  
20 result is due to the components that are reset by glitch 200 in  
21 performing their programmed operations after being reset. Thus,  
22 the reset triggered by the glitch 200 results in mistiming that  
23 leads to the locking in graphics chip 125 when the actual  
24 subsequent reset portion 205 is received by the components of



1 the graphics chip 125. It is understood that the audio chip 130  
2 and any other chip coupled to the bus 135 is also subject to  
3 negative effects of the glitch 200 as described above.

4 Figure 3 is a schematic block diagram of a system 300 that  
5 is capable of compensating for glitches in a reset signal, in  
6 accordance with an embodiment of the present invention. The  
7 system 300 may include a graphics chip 305 and/or an audio chip  
8 310 and/or other types of chip 315. The graphics chip 305,  
9 audio chip, and other chip 315 are coupled via a bus 320 to the  
10 chipset 105. The bus 320 may be, for example, a PCI bus. In  
11 Figure 3, additional chips may also be coupled to (or may  
12 instead be coupled to) the bus 320, or only one or some of the  
13 graphics chip 305, audio chip 310, or other chip 315 may be  
14 coupled to the bus 320.

15 In one embodiment, the present invention provides a reset  
16 circuit 325 which compensates for glitch occurrence in a reset  
17 signal 330. For purposes of explaining the functionality of the  
18 present invention, the reset circuit 325 is shown as being  
19 included in the graphics chip 305. However, other reset  
20 circuits in accordance with an embodiment of the present  
21 invention may also be included in the audio chip 310, in the  
22 other chip 315 and/or in other integrated circuits that may be  
23 coupled to the bus 320. For example, the audio chip 310 may  
24 include a reset circuit 350 in accordance with an embodiment of

1 the present invention. The other chip 315 may include a reset  
2 circuit 355 in accordance with an embodiment of the present  
3 invention.

4 It is also noted that in the embodiment shown in Figure 3,  
5 the reset circuit 325 is shown as being an internal component of  
6 the graphics chip 305. However, the reset circuit 325 may also  
7 be external to the graphics chip 305 or may be a separate module  
or component that is coupled to the graphics chip 305.

Similarly, the reset circuit 350 may also be external to the  
audio chip 310 or may be a separate module or component that is  
coupled to the audio chip 310. The reset circuit 355 may also  
be external to the other chip 355 or may be a separate module or  
component that is coupled to the other chip 355.

In Figure 3, the reset circuit 325 has an input coupled to  
an input/output (I/O) interface 335 for receiving the reset  
signal 330 in the graphics chip 305. The reset circuit 325  
17 generates output reset signals which reset all appropriated  
18 components in the graphics chip 305. Similarly, the reset  
19 circuit 350 generates output reset signals which reset all  
20 appropriate components in the audio chip 310, while the reset  
21 circuit 355 generates reset signals which reset all appropriate  
22 components in the other chip 355. In one embodiment, the reset  
23 circuit 325 uses a set/reset (S-R) flop to recognize the exact  
24 state of the reset signal 330. For purposes of explaining the

1 functionality of the invention, only the function of the reset  
2 circuit 325 is explained in detail. It is understood, however,  
3 that the reset circuits 350 and 355 function in a manner similar  
4 to the reset circuit 325.

5 Figure 4 is a schematic circuit diagram of one embodiment  
6 of the reset circuit 325 of Figure 3. The reset circuit 325a  
7 compares the original reset signal 330 with a delayed version of  
the reset signal 330. When the reset circuit 325a detects both  
the original non-delayed reset signal 330 and the delayed  
version of the reset signal 330 to be in the same state, then  
that state (which is output from the S-R flop) is applied to the  
appropriate components of the graphics chip 305.

In the embodiment illustrated in Figure 4, the reset  
circuit 325a includes a NAND gate 400 and a NOR gate 405. The  
output of the NAND gate 400 is coupled to a set-reset (S-R) flop  
410 which has an output coupled to a buffer 415. The output of  
NOR gate 405 is coupled to an inverter 420 which has an output  
coupled to the S-R flop 410. In one embodiment, the S-R flop  
410 includes a NAND gate 425 and a NAND gate 430. The NAND gate  
425 has a first input coupled to the output of the NAND 400.  
The output of the NAND gate 425 is coupled to the input of the  
buffer 415. The NAND gate 430 has a first input coupled to the  
output of the NAND gate 425 and a second input coupled to the

1 output of the inverter 420. The output of NAND gate 430 is  
2 coupled to the second input of NAND gate 425.

3 The reset circuit 325a uses the S-R flop 410 to recognize  
4 the exact state of a reset signal. The reset signal is delayed  
5 and then compared with the original, non-delayed reset signal.  
6 When both the delayed reset signal and the original, non-delayed  
7 reset signal are in the same state (asserted state or un-  
8 asserted state), a set or a reset occurs in the S-R flop 410.  
9 The output of the S-R flop 410 is fed to all appropriate  
10 circuits and components in an integrated circuit that implements  
11 the reset circuit 325a.

12 Various features in Figure 4 may be modified in accordance  
13 with an embodiment of the present invention. For example, the  
14 inverter 420 may be omitted and the NOR gate 405 may be replaced  
15 with an OR gate. Other modifications may be appropriately made  
16 for the embodiment disclosed in Figure 4.

17 Reference is now made to the reset circuit 325a in Figure 4  
18 and the timing diagrams in Figures 5 and 6 for purposes of  
19 describing the functionality of one embodiment of the present  
20 invention. The following logic operations shown in Tables 1 and  
21 Table 2 also apply to the appropriate logic components shown in  
22 Figure 4.

23

24

1 Table 1: NAND Operation

Input A	Input B	Output QN
0	0	1
0	1	1
1	0	1
1	1	0

2

3 Table 2: NOR Operation

Input A	Input B	Output QN
0	0	1
0	1	0
1	0	0
1	1	0

TOP SECRET

Figure 5 illustrates various waveform diagrams of the signals that are processed by the reset circuit of Figure 3. The waveform diagrams include an incoming reset signal GFRST\_IN0 which is the digitized version of the incoming reset signal 330 of Figure 3. The initial portion of the reset signal GFRST\_IN0 is shown, with the reset signal GFRST\_IN0 switching from a low state to a high state. Figure 6 illustrates the remaining portion of the reset signal GFRST\_IN0, with the reset signal GFRST\_IN0 switching from a high state to a low state. Thus, Figures 5 and 6 show the entirety of one example of a reset signal GFRST\_IN0 and the entirety of one example of the glitch free output (GFRST\_Q) of a reset circuit that is used to reset the appropriate component in an integrated circuit such as graphics chip 305 (Figure 3).



1       The GFRST\_IN0 reset signal is the incoming reset signal  
2       that is generated from the chipset 105 and transmitted across  
3       the bus 320 to graphics chip 305 and to other integrated  
4       circuits that may be coupled to the bus 320 (such as audio chip  
5       310 and/or other chips 315). The GFRST\_IN0 reset signal is  
6       received by the first input of NAND gate 400 and by the first  
7       input of NAND gate 405.

8       The GFRST\_IN100 delayed reset signal is a delayed version  
9       of the GFRST\_IN0 reset signal. In one embodiment, a delay stage  
10       450 is used to delay the GFRST\_IN0 reset signal to generate the  
11       GFRST\_IN100 delayed reset signal. The delay stage 450 may be  
12       formed by, for example, one-hundred delay elements in an array.  
13       The delay stage 450 may be located in, for example, in the reset  
14       circuit 325 or in the I/O buffer 335 (Figure 3). Other numbers  
15       of delay elements in the array may be implemented in the delay  
16       stage 450 in order to vary the delay period of the GFRST\_IN100  
17       delayed reset signal.

18       During initial time t1, the GFRST\_IN0 reset signal and the  
19       GFRST\_IN100 delayed reset signal are at a low level. The  
20       GFRST\_IN0 and GFRST\_IN100 are received by both the NAND gate 400  
21       (Figure 4) and the NOR gate 405. In response to the low level  
22       GFRST\_IN0 reset signal and GFRST\_IN100 reset signal, the NAND  
23       gate 400 outputs a GFRST\_SET signal at a high level. In  
24       response to the low level GFRST\_IN0 reset signal and GFRST\_IN100

1 reset signal, the NOR gate 405 outputs a GFRST\_RESETB signal at  
2 a high level. The high level GFRST\_RESETB signal is inverted by  
3 the inverter 420 into a low level GFRST\_RESET signal. The high  
4 level GFRST\_SET signal and the low level GFRST\_RESET signal is  
5 received by the S-R flop 410. The S-R flop 410 outputs a low  
6 GFRST\_QFB signal, which the buffer 415 delays as the reset  
7 circuit output signal GFRST\_Q. This reset circuit output signal  
8 is applied to the appropriate components of an integrated  
9 circuit such as graphics chip 305 (Figure 3).

10 At time t2, a glitch 500 occurs in the GFRST\_IN0 incoming  
11 reset signal, and the glitch 500 is delayed by the array 450, as  
12 shown at time t3 in the GFRST\_IN100 delayed reset signal. At  
13 time t4, the edge 505 in the GFRST\_IN0 signal occurs as the  
14 GFRST\_IN0 signal switches from a low level to a high level.  
15 This edge 505 is delayed by the array 450 as shown in the  
16 GFRST\_IN100 delayed reset signal.

17 When the GFRST\_IN0 and GFRST\_IN100 signals both switch  
18 high, the GFRST\_SET signal will switch to a low level, as shown  
19 by edge 510 at time t5. When the GFRST\_SET signal switches to a  
20 low level, the GFRST\_QFB signal will switch to a high level as  
21 shown by edge 515. This edge 515 is delayed by buffer 415, as  
22 shown in the GFRST\_Q signal during time t6. The high level  
23 GFRST\_Q signal is applied to all appropriate components in the  
24 integrated circuit (e.g., graphics chip 305) as a reset signal.

1 As shown in Figure 5, the GFRST\_Q signal does not have glitch  
 2 occurrence. Thus, the reset circuit 325a (Figure 4)  
 3 advantageously compensates for glitches that may occur in the  
 4 GFRST\_IN0 incoming reset signal and enables the generation of  
 5 the glitch free signal GFRST\_Q which is applied to appropriate  
 6 components in an integrated circuit.

7 Table 3 shows some input and output values for the S-R flop  
 410 at successive times ( $T_n$ ,  $T_{n+1}$ ,  $T_{n+2}$ , and  $T_{n+3}$ , and so  
 forth). These values show when the GFRST\_QFB output value of  
 the S-R flop 410 switches from a low level to a high level.

Table 3: Operation of S-R Flop 410 (when the reset signal  
 switches to high

NAND 425 INPUT A (GFRST_SET)	NAND 425 INPUT B (NAND 430 OUTPUT QN)	NAND 425 OUTPUT QN (GFRST_QFB)	NAND 430 INPUT A (NAND 425 OUTPUT QN)	NAND 430 INPUT B (GFRST_RESET)	NAND 430 OUTPUT QN
( $T_n$ ) 1	( $T_n$ ) 1	( $T_{n+1}$ ) 0	( $T_n$ ) X	( $T_n$ ) 0	( $T_n$ ) 1
( $T_{n+2}$ ) 1	( $T_{n+2}$ ) 1	( $T_{n+3}$ ) 0	( $T_{n+2}$ ) 0	( $T_{n+2}$ ) 1	( $T_{n+2}$ ) 1
( $T_{n+4}$ ) 0	( $T_{n+4}$ ) 1	( $T_{n+5}$ ) 1	( $T_{n+4}$ ) 0	( $T_{n+4}$ ) 0	( $T_{n+4}$ ) 1
( $T_{n+6}$ ) 0	( $T_{n+6}$ ) 1	( $T_{n+7}$ ) 1	( $T_{n+6}$ ) 1	( $T_{n+6}$ ) 1	( $T_{n+6}$ ) 0

15 X = don't care value

16

17 It is noted further that the delay applied to the GFRST\_IN0  
 18 incoming reset signal can be minimized to compensate for small  
 19 glitches in the GFRST\_IN0 incoming reset signal. The delay  
 20 applied to the GFRST\_IN0 incoming reset signal can be increased

1 to compensate for larger glitches in the GFRST\_IN0 incoming  
2 reset signal.

3 Figure 6 illustrates various waveform diagrams of the  
4 signals that are processed by the reset circuit of Figure 3,  
5 with the GFRST\_IN0 incoming reset signal shown as switching to a  
6 low state. At time t10, the GFRST\_IN0 incoming reset signal is  
7 still at a high level. At time t11, the GFRST\_IN0 incoming  
8 reset signal switches to a low level as shown by the edge 600 at  
9 time t11. This edge 600 is delayed by the array 450 as shown by  
10 the edge 600 in GFRST\_IN100 delayed incoming reset signal.

11 It is noted that when the GFRST\_RESET signal will switch to  
12 a low level as shown by edge 610. The low GFRST\_RESET signal  
13 will cause the output of NAND 430 to switch to a high level.  
14 When the GFRST\_SET signal and the output of NAND 430 are both at  
15 a high level, then the GFRST\_QFB output of NAND 425 will switch  
16 to a low level, as shown by edge 615 at time t12. The edge 615  
17 is delayed by buffer 415 as shown by the edge 615 in the GFRST\_Q  
18 signal at time t12. Thus, after time t12, the GFRST\_Q signal  
19 (which is applied as the reset signal to the components of an  
20 integrated circuit) will be at a low level.

21 At time t13, a glitch 605 may occur in the GFRST\_IN0  
22 incoming reset signal. The delay applied to the GFRST\_IN0  
23 glitch and the various components of reset circuit 325  
24 (including S-R flop 410) permit the GFRST\_Q signal to remain at

1 a low level even if the glitch 605 occurs in the GFRST\_IN0  
2 incoming reset signal.

3 Table 4 shows some input and output values for the S-R flop  
4 410 at successive times (Tn+10, Tn+11, Tn+12, and Tn+13, and so  
5 forth). These values show when the GFRST\_QFB output value of  
6 the S-R flop 410 switches from a high level to a low level.

7

Table 4: Operation of S-R Flop 410 (when the reset signal  
switches to high)

NAND 425 INPUT A (GFRST_SET)	NAND 425 INPUT B (NAND 430 OUTPUT QN)	NAND 425 OUTPUT QN (GFRST_QFB)	NAND 430 INPUT A (NAND 425 OUTPUT QN)	NAND 430 INPUT B (GFRST_RESET)	NAND 430 OUTPUT QN
(Tn+10) 0	(Tn+10) X	(Tn+11) 1	(Tn+10) 1	(Tn+10) 1	(Tn+10) 0
(Tn+12) 1	(Tn+12) 0	(Tn+13) 1	(Tn+12) 1	(Tn+12) 1	(Tn+12) 0
(Tn+14) 1	(Tn+14) 0	(Tn+15) 1	(Tn+14) 1	(Tn+14) 0	(Tn+14) 1
(Tn+16) 1	(Tn+16) 1	(Tn+17) 0	(Tn+16) 1	(Tn+16) 0	(Tn+16) 1

X = don't care value

Figure 7 illustrates various example waveform diagrams as a  
14 function of voltage (volts) versus time (seconds). The  
15 GFRST\_IN0 incoming reset signals may include glitches 700, 705,  
16 710, and 715. The waveform signal 730 is the digitized form of  
17 the GFRST\_IN0 incoming reset signal. The signal 730 may be  
18 digitized by, for example, the input/output buffer 335 (Figure  
19 3). As shown in Figure 7, the digitized waveform signal  
20 (GFRST\_IN0) includes glitches 700', 710', and 715' which are due  
21 to the glitches 700, 710, and 715, respectively. The reset

1 circuit 325a (Figure 4) permits the glitch free signal GFRST\_Q  
2 to be generated and to be applied as a reset signal to  
3 appropriate components in an integrated circuit.

4 As further shown in Figure 7, the reset circuit permits the  
5 glitches 700 and 705 (occurring before the high state portion  
6 740) and the glitches 715 and 715 (occurring after the high  
7 state portion 740) to be filtered. As a result, glitches will  
not occur before and after the high portion 750 of the GFRST\_Q  
signal.

Figure 8 is a flowchart diagram of a method of compensating  
for glitch occurrence in an incoming reset signal, in accordance  
with an embodiment of the present invention. An incoming signal  
is first received (800), with the incoming signal having at  
least one glitch occurrence. For example, this incoming signal  
may be the GFRST\_IN0 digitized incoming reset signal in Figure  
16 4. The incoming signal is also delayed (805) to produce a  
17 delayed signal. For example, the incoming signal may be delayed  
18 by delay stage 450 (Figure 4) to produce the GFRST\_IN100 delayed  
19 incoming reset signal. A first logic operation is performed  
20 (810) on the incoming signal and the delayed signal to generate  
21 an input set flop signal. A second logic operation is performed  
22 (815) on the incoming signal and the delayed signal to generate  
23 an input reset flop signal. The performed logic operations  
24 (810) and (815) may be performed substantially at the same time.

1 As an example, the first logic operation is performed (810) on  
2 the GFRST\_IN0 signal and the GFRST\_IN100 delayed signal by the  
3 NAND gate 400 (Figure 4) to generate the GFRST\_SET input set  
4 flop signal, while the second logic operation is performed (815)  
5 on the GFRST\_IN0 signal and the GFRST\_IN100 delayed signal by  
6 the NOR gate 405 (Figure 4) to generate the GFRST\_RESETB signal.  
7 In one embodiment, the GFRST\_RESETB signal is inverted by  
8 inverter 420 to generate the GFRST\_RESET input reset flop  
signal.

A third logic operation is then performed (820) on the  
input set flop signal and the input reset flop signal to  
generate a reset signal without a glitch. For example, the  
third logic operation is performed (820) on the GFRST\_SET input  
set flop signal and the GFRST\_RESET input reset flop signal by  
the S-R flop 410 (Figure 4) to generate the GFRST\_QFB reset  
signal without a glitch occurrence. The GFRST\_QFB reset signal  
17 can be applied (825) to at least some portion of an integrated  
18 circuit as a reset signal. In one embodiment, the GFRST\_QFB  
19 reset signal is buffered by the buffer 415 (Figure 4) to  
20 generate the GFRST\_Q buffered reset signal which is applied to  
21 at least some portion of an integrated circuit as a reset  
22 signal.

23 Figure 9 illustrates another embodiment of a reset circuit  
24 of Figure 3. The reset circuit (sample-hold circuit) 325b



1 receives an incoming reset signal "reset" and delays an incoming  
2 reset signal to generate a delayed reset signal "delayed\_reset".  
3 The sample-hold circuit 325b compares the delayed\_reset delayed  
4 reset signal with the non-delayed reset signal. When both the  
5 non-delayed reset signal and the delayed\_reset signal are the  
6 same state (asserted or non-asserted), then the non-delayed reset  
7 signal is sampled as the output value "OUTB". On the other hand,  
8 if the non-delayed reset signal and the delayed\_reset signal are  
9 not the same state, then the non-delayed reset signal is not  
10 sampled, and the previously sampled state of the non-delayed  
11 reset signal is held at the output value "OUTB".

12 In one embodiment, the reset circuit (sample-hold circuit)  
13 325b includes an XNOR gate 900, a delay stage (e.g., array) 905,  
14 an inverter 910, an optional XOR gate 915, a pass-through  
15 circuit 920, and inverters 925 and 930. The pass-through  
16 circuit 920 includes N-channel transistor 935 and P-channel  
17 transistor 940.

18 Reference is now made to the reset circuit 325b in Figure 9  
19 and the timing diagrams in Figure 10. The following logic  
20 operations shown in Tables 5 and Table 6 also apply to the  
21 appropriate logic components shown in Figure 9.

22  
23  
24



1 Table 5: XOR Operation

Input A	Input B	Output QN
0	0	0
0	1	1
1	0	1
1	1	0

2

3 Table 6: XNOR Operation

Input A	Input B	Output QN
0	0	1
0	1	0
1	0	0
1	1	1

4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18

The delay element 905 delays the incoming "reset" signal as the delayed signal "delayed\_reset". Thus, a glitch 1000 in the reset signal will be shown as the delayed glitch 1000 in the delayed\_reset signal. Similarly, the positive pulse 1005 in the incoming reset signal will also be delayed as shown in the delayed\_reset signal. Similarly, a glitch 1010 that may occur in the incoming reset signal will also be delayed as shown in the delayed\_reset signal. The XNOR gate 900 output signal, XNOR\_OUT, is determined by the logic operation shown in Table 6. Thus, when both of the reset signal and the delayed\_reset signal are in the same state (e.g., when the reset signal and the delayed\_reset signal are both low, or when the reset signal and the delayed\_reset signal are both high), then the XNOR\_OUT value will be high. The interval when the XNOR\_OUT value is high is

1 indicated by "s" in Figure 10. When both of the reset signal  
2 and the delayed\_reset signal are in opposite states (e.g., when  
3 the reset signal is high and the delayed\_reset signal is low; or  
4 when the reset signal is low and the delayed\_reset signal is  
5 high), then the XNOR\_OUT value will be low. The interval when  
6 the XNOR\_OUT value is low is indicated by "h" in Figure 10.

7 When XNOR\_OUT is high, then the N-channel transistor 935 is  
8 on because the gate of transistor 935 is receiving the high  
XNOR\_OUT signal. The high XNOR\_OUT signal is also inverted by  
the inverter 910 into a low inverted\_XNOR\_OUT signal that turns  
on the P-channel transistor 940. Since both of the transistors  
935 and 940 are on, the pass-through circuit 920 will pass  
through the reset signal. Thus, the value of the reset signal  
is sampled (as indicated by "s") and will be the value of OUTB  
signal.

1 When XNOR\_OUT is low, then the N-channel transistor 935 is  
17 off because the gate of transistor 935 is receiving the low  
18 XNOR\_OUT signal. The low XNOR\_OUT signal is also inverted by  
19 the inverter 910 into a high inverted\_XNOR\_OUT signal that turns  
20 off the P-channel transistor 940. Since both of the transistors  
21 935 and 940 are off, the pass-through circuit 920 will not pass  
22 through the reset signal. Thus, the current value of the reset  
23 signal will be held (as indicated by "h") and will be the value  
24 of OUTB signal.

1 As shown in Figure 10, the OUTB signal properly remains low  
2 if a glitch 1000 or 1010 occurs in the reset signal. The OUTB  
3 signal properly goes high when the positive pulse 1005 of the  
4 reset signal is received by the reset circuit 325b.

5 In one embodiment, the XOR gate 915 serves to add  
6 additional delay to the reset signal to set the timing of  
7 arrival to the pass-through circuit 920 of the XNOR\_OUT signal,  
8 the inverted\_XNOR\_OUT signal, and the reset signal.

Figure 11 is a flowchart diagram of a method of  
compensating for glitch occurrence in an incoming reset signal,  
in accordance with another embodiment of the present invention.  
An incoming signal is first received (1100), with the incoming  
signal having at least one glitch occurrence. For example, this  
incoming signal may be the "reset" signal in Figure 10. The  
incoming signal is also delayed (1105) to produce a delayed  
signal. For example, the incoming signal may be delayed by  
17 array 905 (Figure 10) to produce the "delayed\_reset" signal.  
18 The following operation is then performed (1110) where the  
19 incoming signal value is sampled when the incoming signal and  
20 the delayed signal are in the same state, and where the previous  
21 value of the incoming signal is held when the incoming signal  
22 and the delayed signal are in the opposite state. For example,  
23 an XNOR gate 900 and a pass-through circuit 935 are used for  
24 sampling the values of and/or holding the previous values of the

1 incoming signal. Based on the sampled values of the incoming  
2 signal and the held values of the incoming signal, a signal is  
3 then generated (1115) for use as a reset signal for at least  
4 some portion of an integrated circuit.

5 The reset circuits described above are very versatile and  
6 can be used in any portion of a circuit board to compensate for  
7 glitches in the reset signals. For example, a reset circuit in  
8 accordance with an embodiment of the invention can be implemented  
9 internally to an integrated circuit or may be implemented  
10 externally to an integrated circuit. Other variations and  
11 modifications of the above-described embodiments and methods are  
12 possible in light of the foregoing teaching.

13 Further, at least some of the components of this invention  
14 may be implemented by using a programmed general purpose digital  
15 computer, by using application specific integrated circuits or  
16 field programmable gate arrays, or by using a network of  
17 interconnected components and circuits, and/or by use of  
18 discrete elements.

19 It is also within the scope of the present invention to  
20 implement a program or code that can be stored in an  
21 electronically-readable medium to permit a computer to perform  
22 any of the methods described above.

23 The above description of illustrated embodiments of the  
24 invention, including what is described in the Abstract, is not

1 intended to be exhaustive or to limit the invention to the  
2 precise forms disclosed. While specific embodiments of, and  
3 examples for, the invention are described herein for  
4 illustrative purposes, various equivalent modifications are  
5 possible within the scope of the invention, as those skilled in  
6 the relevant art will recognize.

7       These modifications can be made to the invention in light  
8 of the above detailed description. The terms used in the  
following claims should not be construed to limit the invention  
to the specific embodiments disclosed in the specification and  
the claims. Rather, the scope of the invention is to be  
determined entirely by the following claims, which are to be  
construed in accordance with established doctrines of claim  
interpretation.